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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re the Application of:

Ming ZHANG et al.	Art Unit: 2838
Application No.: 10/522,738	Examiner: Jeffrey L. STERRETT
Filed: October 7, 2005	Attorney Dkt. No.: 11016-0035

For: VOLTAGE-VOLTAGE CONVERTER FOR INTEGRATED CIRCUITS

INFORMATION DISCLOSURE STATEMENT

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

November 7, 2006

Sir:

In accordance with the provisions of 37 C.F.R. 1.56, 1.97 and 1.98, the attention of the Patent and Trademark Office is hereby directed to the references listed on the attached form PTO-1449. It is respectfully requested that the references be expressly considered during the prosecution of this application, and that the references be made of record therein and appear among the "References Cited" on any patent to issue therefrom.

For the Examiner's information, Document 1 is listed on Page 1, Line 27 of the Specification; Document 2 is listed on Page 1, Line 29 of the Specification; and Document 3 is listed on Page 1, Line 10 of the Specification.

Applicants respectfully submit that this disclosure is being made before the mailing of a first Office Action on the merits, hence, no fee is required, however, please charge any fee deficiency or credit any overpayment to Deposit Account No. 50-1088.

Respectfully submitted,
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FORM PTO-1449 U.S. DEPARTMENT OF COMMERCE PATENT AND TRADEMARK OFFICE	ATTY. DOCKET NO.	SERIAL NO.
	11016-0035	10/522,738
LIST OF REFERENCES CITED BY APPLICANT	APPLICANT	
	Ming ZHANG et al.	
(Use several sheets if necessary)	FILING DATE	GROUP ART UNIT
	October 7, 2005	2838

U.S. PATENT DOCUMENTS

EXAMINER INITIAL		DOCUMENT NO.	DATE	NAME	CLASS	SUB-CLASS	FILING DATE

FOREIGN PATENT DOCUMENTS

		DOCUMENT NO.	DATE	COUNTRY	CLASS	SUB-CLASS	TRANSLATION YES	NO	PART.
	1.	WO 02/43232	5/2002	WIPO			X		

OTHER REFERENCES *(Including Author, Title, Date, Pertinent Pages, Etc.)*

	2.	**XP-02241539: "An Experimental 1.5V 64-Mb DRAM" by Yoshinobu Nakagome, et al. IEEE Journal of Solid-State Circuits, Vol. 26, No. 4; pages 465-472; April 1991.**
	3.	**"On-Chip High-Voltage Generation in MNOS Integrated Circuits Using an Improved Voltage Multiplier Technique" by John F. Dickson. IEEE Journal of Solid-State Circuits, Vol. SC-11, No. 3; pages 374-378; June 1976.**

EXAMINER	DATE CONSIDERED

*EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609; Draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.